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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/607,584

06/29/2000

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81862.P183

9074

7590

08/05/2004

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EXAMINER

JAROENCHONWANIT, BUNJOB

ART UNIT

PAPER NUMBER

2143

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,584	WILFORD ET AL.	
	Examiner	Art Unit	
	Bunjob Jaroenchonwanit	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-13,15-21 and 23-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9-13,15-21 and 23-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06/29/00 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/8/04 has been entered.
2. Applicant's arguments with respect to claims 1-7, 9-13, 15-21 and 23-29 have been considered but are moot in view of the new ground(s) of rejection.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of using statistics information included cell count per channel and CLP count to generate interrupt signal from counter to CPU to indicate high priority as claimed in claims 3, 9, 15 and 24 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
5. Claims 3, 9, 15 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The aforementioned claims are dependent claims of claim 1, 7, 13 and 21, respectively. Interpretation of such dependent claims, the consideration of all parent claims'

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limitations must be incorporated, in this instance, the interpretation found insufficient support in the specification that the Cell count and CLP count were used to generate interrupt signal, which is being used for priority order indication. In contrary, the specification supported using LCI count for generate interrupt signal from FIFO to CPU, which in turn indicating priority order (see inter alia specification page 14, paragraph 2). Furthermore, the specification inadequately described the nexus between Cell, CLP counts and LCI count, in such full clear and concise manner to enable one ordinary skilled in the art to, without undue experimentation, transform the CLP and cell count per VC value to control interrupt signal that is used to for priority indication as claimed therein.

6. Claims 3, 9, 15 and 23 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure, which is not enabling. How to used the statistical information as claimed in their independent claims to generate interrupt signal for priority indication, which are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

7. The specification is objected to under 35 U.S.C. 112, first paragraph, as failing to adequately teaches how to make/or use the invention, i.e., failing to disclose how to generate interrupt signal from statistic information as defined in their parent claims , i.e., cell count per channel and CLP count.

8. Applicant's disclosure is insufficient to allow one of ordinary skill in the art to make or use the invention without undue experimentation because applicant did not adequately disclose the necessary apparatus to perform the claimed method. See *In re Gunn*, 190 USPQ 402, 406

(CCPA 1976.) In fact applicant's disclosure did not even suggest nor implied the use of cell count and CLP count for such functionality.

9. Claim 3, 9, 15 and 23 are rejected under 35 U.S.C. 112, first paragraph, for reason set forth in the objection to the specification.

10. It is suggested that applicant could overcome 112/first paragraph rejection by providing a suitably detailed that linked the CLP and Cell Count per VC with LCI, and system diagram (with appropriate cross-indexing in the detailed description to reference numerals on said system diagrams.) No new matter should be added.

11. The text of those sections of Title 35, U.S. Code 112 second paragraph and 103 not included in this action can be found in a prior Office action.

12. Claims 1, 7, 13 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear, "a count value" and "the count value" recited in the claims are referred, thereto.

13. Claims 1-29 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cielsak et al (US. 5,402,416) and Yoshimura et al. (US. RE37,435).

14. Regarding claims 1, 2, 7, 8, 13, 14, 21, 22 and 27 Cielsak discloses a network interface comprising:

a memory to store statistics for a connection; a counter, to count statistic stored in the memory (counting switch stabilizing message, Col. 9, lines 29-53);

a processor to determine if a count value of connections is above a threshold (block 120, Fig. 9) and to collect the statistics for the connections of the switch stored in the memory derived

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from counters having a counter value above the threshold (block 122 fig 9) before collecting statistics in the memory derived from counters having a count value below the threshold (block 126, Fig.9; Col. 13, lines 15-39). Cielsak does not explicitly disclose the statistic includes a number of cells per virtual channel and a number of cells having loss priority bit. However, in the same field of endeavor, Yoshimura discloses a supervisory control system for controlling cells transmission over ATM switching system. Yoshimura's teaching included connection modification based on cells count in Virtual Channel and Cell Loss Priority (CLP) counting and threshold comparison (See inter alia Fig.3-7, Col.1, lines 25-34; Col.4, lines 11-25; Col. 6, line 29-Col. 7, line 6). It would have been obvious to one of ordinary skilled in the art at the time of the invention was made to incorporate the teaching of using the result of counting cells in a virtual channel and counting of cell loss priority as suggested by Yoshimura for controlling network traffic, establishing connection and other purpose in Cielsak in order to improve quality of network traffic.

15. Regarding claims claim 27, in addition to, the claims are analogous in context, the additional limitations, e.g., CPU, counter, internal counter, are inherent limitations, since CPU and counter are required for such operation and computations. Thus claim 27 is rejected by the same rationale set forth above.

16. Referring to claims 3, 9, 15 and 23, Cielsak discloses sending an interrupt signal when having a determined count value above the threshold (the stable state triggering signal, Cielsak, Col. 13, lines 22-30).

17. Referring to claims 4, 10, 16 and 24, Cielsak-Yoshimura discloses collecting statistics from counters with corresponding interrupt signals before other counters with no corresponding

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interrupt signals (an interrupt signal is generated from switch in response to a count value > threshold, before proceed to determine whether the count value is less than threshold, inherently, information, e.g., statistic, must be collected from before the one with less value, Cielsak, Col. 13, lines 22-30).

18. Regarding claim 19, Cielsak-Yoshimura discloses its switch has multiple ports (Cielsak Fig. 2).

19. Regarding claims 5, 6, 11, 12, 17, 18, 25 and 26, Cielsak-Yoshimura discloses the invention substantially, as claimed, as described in their base claims, including enter stable state, which include logical; identifier in buffer, table (Cielsak, Fig. 9, message includes identification, Col. 8, lines 15-17; Col. 9, lines 49-52; Col. Table 1 Col. 10). Despite the fact that Cielsak-Yoshimura is silent to the buffer used for storing connection identification is a FIFO type. However, it teaches the FIFO is used in the network for queuing purpose (Cielsak, Col. 3, lines 20-34). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to used the FIFO for storing connection Identification, with the motivation of Queuing stable ports for selectively connections.

20. Regarding claim 20, Cielsak-Yoshimura discloses the invention substantially as claimed, as described in claim 19, but fails to include using OC ports, STS ports and SDH ports. Official Notice (see MPEP ' 2144.03 Reliance on "Well Known" Prior Art) is taken that OC ports, STS ports and SDH ports were well known in the art and have been used for forwarding and receiving data in network devices. Thus, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to expand Cielsak-Yoshimura design concept to cover other

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types of network port, including OC ports, STS ports and SDH ports, with the motivation of increasing flexibility and applicability and competitiveness of the system.

21. Regarding claim 28, Cielsak-Yoshimura discloses the invention substantially, as claimed, as described, including in claim 27, but fails to explicitly state that the CPU counters are wider than the module counters. It is inherent that a CPU has a fixed size for its internal counters, which depends only on the type of processor available in the market at a specific time of purchase. To choose a module (external) counter of smaller size would be intuitive in this type of operation because it would minimize CPU read cycle. Obtaining information from smaller external counters would require less machine cycle than obtaining information from external counters larger than CPU internal counters. It would have been obvious to one of ordinary skill in the art, at the time of the applicant's invention that choosing a smaller size for the module (external) counters would have been a matter of design choice, in order to expedite processing time.

22. Claim 29 is rejected based on the same analysis for claim 28. The CPU's internal counter size of 64-bits is an inherent characteristic of the CPU. Setting the module counter size to 32-bits would be intuitive because it would reduce the time necessary to transfer data to the CPU. It would have been obvious to one of ordinary skill in the art, at the time of the applicant's invention that choosing a size of 32-bits for the module (external) counters would have been a matter of design choice, in order to expedite processing time.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bunjob Jaroenchonwanit whose telephone number is (703) 305-9673. The examiner can normally be reached on 8:00-17:00. If attempts to reach the examiner

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by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on (703) 308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'B. Jaroenchonwanit', with a stylized flourish at the end.

Bunjob Jaroenchonwanit
Primary Examiner
Art Unit 2143

/bj
8/2/04